

STS12NF30L

N-channel 30V - 0.008Ω - 12A SO-8 STripFET™ II Power MOSFET

Features

Туре	V _{DSS}	R _{DS(on)}	I _D	
STS12NF30L	30V	<0.009Ω	12A	

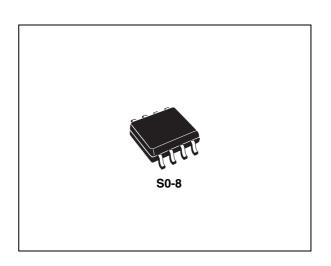
- Standard outline for easy automated surface mount assembly
- Low threshold drive

Description

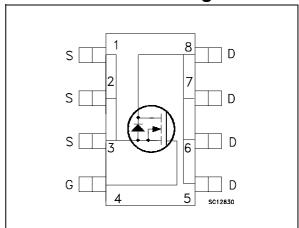
This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature SizeTM" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

Application

■ Switching application



Internal schematic diagram



Order code

Part number	Marking	Package	Packaging
STS12NF30L	S12NF30L	SO-8	Tape & reel

Contents STS12NF30L

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STS12NF30L Electrical ratings

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source voltage (v _{gs} = 0)	30	V
V_{GS}	Gate- source voltage	±16	V
I _D	Drain current (continuos) at T _C = 25°C	12	Α
I _D	Drain current (continuos) at T _C = 100°C	7.5	Α
I _{DM} ⁽¹⁾	Drain current (pulsed)	48	Α
P _{TOT}	Total dissipation at T _C = 25°C	2.5	W

^{1.} Pulse width limited by safe operating area

Table 2. Thermal data

R _{thj-a}	Thermal resistance junction-ambient Max	50	°C/W
T_J	Maximum operating junction temperature	150	°C
T _{stg}	Storage temperature	-55 to 150	°C

Electrical characteristics STS12NF30L

2 Electrical characteristics

(T_{CASE} =25°C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter Test conditions		Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0$	30			V
	Zero gate voltage	V _{DS} = Max rating			1	μΑ
I _{DSS}	Drain current (V _{GS} = 0)	V _{DS} =Max rating,T _C =125°C			10	μΑ
I _{GSS}	Gate-body leakage current (V _{DS} = 0)	V _{GS} = ± 16V			±100	nA
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1			٧
R _{DS(on)}	Static drain-source on resistance	$V_{GS} = 10V, I_D = 6A$ $V_{GS} = 4.5V, I_D = 6A$		0.008 0.01	0.009 0.011	Ω Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
g _{fs} ⁽¹⁾	Forward transconductance	V _{DS} = 15V _, I _D =6A		15		S
C _{iss}	Input capacitance			2400		pF
C _{oss}	Output capacitance	$V_{DS} = 25V, f = 1 \text{ MHz}, $ $V_{GS} = 0$		590		pF
C _{rss}	Reverse transfer capacitance	$V_{GS} = 0$		200		pF
Qg	Total gate charge	$V_{DD} = 24V, I_D = 12A,$		35	50	nC
Q_{gs}	Gate-source charge	$V_{GS} = 4.5V$		9		nC
Q_{gd}	Gate-drain charge	(see Figure 13)		18		nC

^{1.} Pulsed: Pulse duration = 300 μ s, duty cycle 1.5.

Table 5. Switching times

Symbol	Parameter Test conditions		Min.	Тур.	Max.	Unit
t _{d(on)}	Turn-on delay time Rise time	V_{DD} =15 V, I_{D} =6A, R_{G} =4.7 Ω , V_{GS} =4.5V (see Figure 12)		35 90		ns ns
t _{d(off)}	Turn-off-delay time Fall time	V_{DD} = 15V, I_D = 6A, R_G = 4.7 Ω , V_{GS} = 4.5V (see Figure 12)		80 35		ns ns
t _{r(Voff)} t _f t _c	Off-voltage rise time fall time cross-over time	V_{DD} =24V, I_{D} =12A, R_{G} =4.7 Ω , V_{GS} =4.5V (see Figure 14)		35 35 80		ns ns ns

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max	Unit
I _{SD}	Source-drain current				12	Α
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)				48	Α
V _{SD} ⁽²⁾	Forward on voltage	$I_{SD} = 12A, V_{GS} = 0$			1.3	V
t _{rr} Q _{rr} I _{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 12A, V_{DD} = 15V$ di/dt = 100A/ μ s, $T_{j} = 150^{\circ}$ C (see Figure 14)		114 456 8		ns nC A

^{1.} Pulse width limited by safe operating area.

^{2.} Pulsed: Pulse duration = $300 \mu s$, duty cycle 1.5%

Electrical characteristics STS12NF30L

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

Figure 2. Thermal impedance

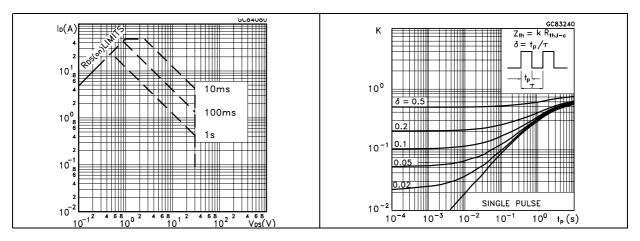


Figure 3. Output characteristics

Figure 4. Transfer characteristics

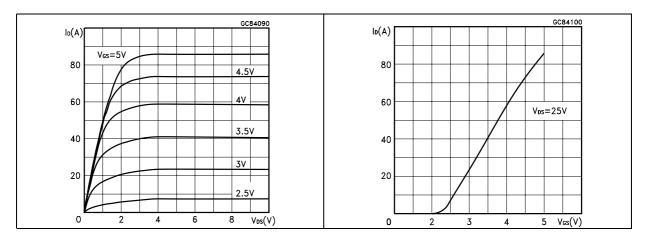
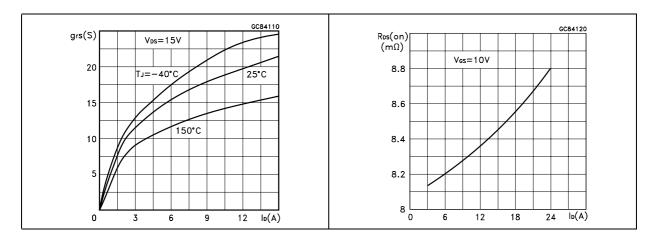


Figure 5. Transconductance

Figure 6. Static drain-source on resistance



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Figure 7. Gate charge vs. gate-source voltage Figure 8. Capacitance variations

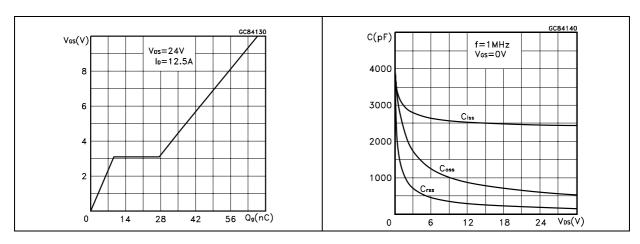


Figure 9. Normalized gate threshold voltage vs. temperature

Figure 10. Normalized on resistance vs. temperature

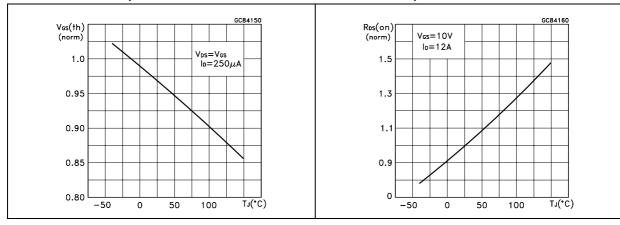
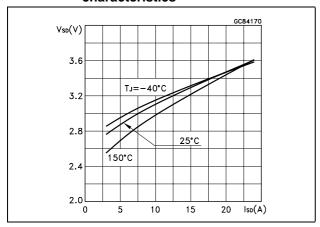


Figure 11. Source-drain diode forward characteristics



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Test circuit STS12NF30L

3 Test circuit

Figure 12. Switching times test circuit for resistive load

Figure 13. Gate charge test circuit

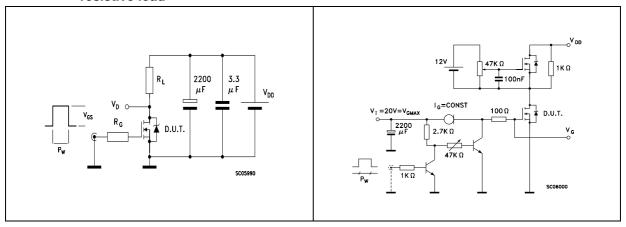


Figure 14. Test circuit for inductive load switching and diode recovery times

Figure 15. Unclamped Inductive load test circuit

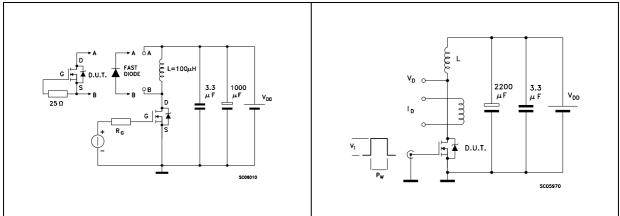
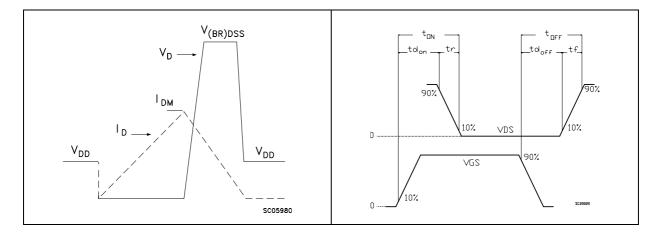


Figure 16. Unclamped inductive waveform

Figure 17. Switching time waveform



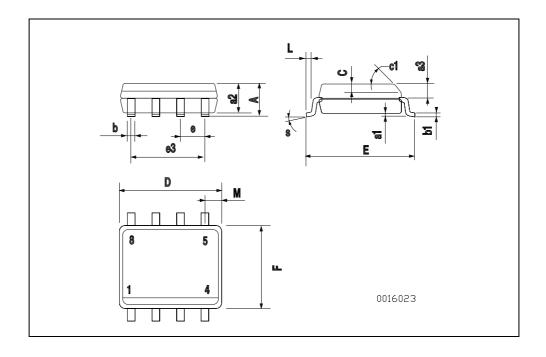
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4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

SO-8 MECHANICAL [DΑ	۱ΤΑ	١
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DIM		mm.			inch	
DIM.	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
Α			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
С	0.25		0.5	0.010		0.019
c1			45 ((typ.)		
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
е		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
М			0.6			0.023
S		•	8 (n	nax.)	•	•



STS12NF30L Revision history

5 Revision history

Table 7. Revision history

Date	Revision	Changes
09-Sep-2004	6	Complete version
17-Aug-2006	7 New template, no content change	
31-Jan-2007	8	Typo mistake on Table 1.
08-May-2007	9	Mistake on <i>Table 6</i>

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